Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	173	703/2.ccls. and @pd>"20050901"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/02/09 10:53
L3	532	(model adj check$3) and @ad<"20020201"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/02/09 10:55
L4	227	L3 and path	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/02/09 10:55

Welcome United States Patent and Trademark Office

□ **Search Results**

BROWSE　　　**SEARCH**　　　**IEEE XPLORE GUIDE**　　　**SUPPORT**

Results for "((model checker<and>path)) <and> (pyr >= 1951 <and> pyr <= 2002)"
Your search matched **175** of **1314030** documents.
A maximum of **500** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

✉ e-mail 🖨 printer friendly

» Search Options

<u>View Session History</u>

<u>New Search</u>

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

((model checker<and>path)) <and> (pyr >= 1951 <and> pyr <= 2002)	**Search ≥**

☐ Check to search only within this results set

Display Format:　◉ Citation　○ Citation & Abstract

⤴ **view selected items**　　**Select All　Deselect All**

View: **1-25** | <u>26-50</u> | <u>51-75</u> | <u>76-100</u> | <u>101-125</u>
| <u>Next ></u>

☐　1. **A language for compositional specification and verification of finite state hardware controllers**
Clarke, E.M., Jr.; Long, D.E.; McMillan, K.L.;
<u>Proceedings of the IEEE</u>
Volume 79, Issue 9, Sept. 1991 Page(s):1283 - 1292
Digital Object Identifier 10.1109/5.97298

<u>AbstractPlus</u> | Full Text: <u>PDF</u>(900 KB)　**IEEE JNL**
<u>Rights and Permissions</u>

☐　2. **Two formal analyses of attack graphs**
Jha, S.; Sheyner, O.; Wing, J.;
<u>Computer Security Foundations Workshop, 2002. Proceedings. 15th IEEE</u>
24-26 June 2002 Page(s):49 - 63
Digital Object Identifier 10.1109/CSFW.2002.1021806

<u>AbstractPlus</u> | Full Text: <u>PDF</u>(534 KB)　**IEEE CNF**
<u>Rights and Permissions</u>

☐　3. **Model checking large software specifications**
Chan, W.; Anderson, R.J.; Beame, P.; Burns, S.; Modugno, F.; Notkin, D.; Reese, J.D.;
<u>Software Engineering, IEEE Transactions on</u>
Volume 24, Issue 7, July 1998 Page(s):498 - 520
Digital Object Identifier 10.1109/32.708566

<u>AbstractPlus</u> | <u>References</u> | Full Text: <u>PDF</u>(488 KB)　**IEEE JNL**
<u>Rights and Permissions</u>

☐　4. **Optimizing symbolic model checking for statecharts**
Chan, W.; Anderson, R.J.; Beame, P.; Jones, D.H.; Notkin, D.; Warner, W.E.;
<u>Software Engineering, IEEE Transactions on</u>
Volume 27, Issue 2, Feb. 2001 Page(s):170 - 190
Digital Object Identifier 10.1109/32.908961

<u>AbstractPlus</u> | <u>References</u> | Full Text: <u>PDF</u>(508 KB)　**IEEE JNL**
<u>Rights and Permissions</u>

☐　5. **Splitting trees and partition refinement in real-time model checking**
Spelberg, R.F.L.; Toetenel, W.J.;
<u>System Sciences, 2002. HICSS. Proceedings of the 35th Annual Hawaii International Conference on</u>
7-10 Jan 2002 Page(s):3996 - 4005

<u>AbstractPlus</u> | Full Text: <u>PDF</u>(1253 KB)　**IEEE CNF**
<u>Rights and Permissions</u>

☐　6. **Three approximation techniques for ASTRAL symbolic model checking of infinite state real-time systems**
Zhe Dang; Kemmerer, R.A.;

Software Engineering, 2000. Proceedings of the 2000 International Conference on
4-11 June 2000 Page(s):345 - 354
Digital Object Identifier 10.1109/ICSE.2000.870425

AbstractPlus | Full Text: PDF(1036 KB)   IEEE CNF
Rights and Permissions

7. **From business process model to consistent implementation: a case for formal verification methods**
Koehler, J.; Tirenni, G.; Kumaran, S.;
Enterprise Distributed Object Computing Conference, 2002. EDOC '02. Proceedings. Sixth International
17-20 Sept. 2002 Page(s):96 - 106
Digital Object Identifier 10.1109/EDOC.2002.1137700

AbstractPlus | Full Text: PDF(365 KB)   IEEE CNF
Rights and Permissions

8. **Probabilistic analysis of anonymity**
Shmatikov, V.;
Computer Security Foundations Workshop, 2002. Proceedings. 15th IEEE
24-26 June 2002 Page(s):119 - 128
Digital Object Identifier 10.1109/CSFW.2002.1021811

AbstractPlus | Full Text: PDF(353 KB)   IEEE CNF
Rights and Permissions

9. **Tree-like counterexamples in model checking**
Clarke, E.; Jha, S.;
Logic in Computer Science, 2002. Proceedings. 17th Annual IEEE Symposium on
22-25 July 2002 Page(s):19 - 29
Digital Object Identifier 10.1109/LICS.2002.1029814

AbstractPlus | Full Text: PDF(446 KB)   IEEE CNF
Rights and Permissions

10. **Application of parametric model checking - the Root Contention protocol**
Bandini, G.; Spelberg, R.L.; de Rooij, R.C.H.; Toetenel, W.J.;
System Sciences, 2001. Proceedings of the 34th Annual Hawaii International Conference on
Jan 3-6 2001 Page(s):10 pp.

AbstractPlus | Full Text: PDF(220 KB)   IEEE CNF
Rights and Permissions

11. **A simple method for extracting models from protocol code**
Lie, D.; Chou, A.; Engler, D.; Dill, D.L.;
Computer Architecture, 2001. Proceedings. 28th Annual International Symposium on
30 June-4 July 2001 Page(s):192 - 203
Digital Object Identifier 10.1109/ISCA.2001.937448

AbstractPlus | Full Text: PDF(176 KB)   IEEE CNF
Rights and Permissions

12. **Formal verification of an IBM coreconnect processor local bus arbiter care**
Goel, A.; Lee, W.R.;
Design Automation Conference, 2000. Proceedings 2000. 37th
June 5-9, 2000 Page(s):196 - 200

AbstractPlus | Full Text: PDF(460 KB)   IEEE CNF
Rights and Permissions

13. **E-process design and assurance using model checking**
Wang, W.; Hidvegi, Z.; Bailey, A.D., Jr.; Whinston, A.B.;
Computer
Volume 33, Issue 10, Oct. 2000 Page(s):48 - 53
Digital Object Identifier 10.1109/2.876292

AbstractPlus | References | Full Text: PDF(212 KB)   IEEE JNL
Rights and Permissions

14. **An industrial view of electronic design automation**
MacMillen, D.; Camposano, R.; Hill, D.; Williams, T.W.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 19, Issue 12, Dec. 2000 Page(s):1428 - 1448

Digital Object Identifier 10.1109/43.898825

AbstractPlus | References | Full Text: PDF(180 KB)   IEEE JNL
Rights and Permissions

15. **Symbolic model checking for self-stabilizing algorithms**
Tsuchiya, T.; Nagano, S.; Paidi, R.B.; Kikuno, T.;
Parallel and Distributed Systems, IEEE Transactions on
Volume 12, Issue 1, Jan. 2001 Page(s):81 - 95
Digital Object Identifier 10.1109/71.899941

AbstractPlus | References | Full Text: PDF(564 KB)   IEEE JNL
Rights and Permissions

16. **An alternative to model checking: verification by random search of AND-OR graphs representing finite-state models**
Owen, D.; Cukic, B.; Menzies, T.;
High Assurance Systems Engineering, 2002. Proceedings. 7th IEEE International Symposium on
23-25 Oct. 2002 Page(s):119 - 126
Digital Object Identifier 10.1109/HASE.2002.1173112

AbstractPlus | Full Text: PDF(1096 KB)   IEEE CNF
Rights and Permissions

17. **Winnowing tests: Getting quality coverage from a model checker without quantity**
Black, P.E.; Ranville, S.;
Digital Avionics Systems, 2001. DASC. The 20th Conference
Volume 2, 14-18 Oct. 2001 Page(s):9B6/1 - 9B6/4 vol.2
Digital Object Identifier 10.1109/DASC.2001.964253

AbstractPlus | Full Text: PDF(253 KB)   IEEE CNF
Rights and Permissions

18. **Bandera: extracting finite-state models from Java source code**
Corbett, J.C.; Dwyer, M.B.; Hatcliff, J.; Laubach, S.; Pasareanu, C.S.; Robby; Hongjun Zheng;
Software Engineering, 2000. Proceedings of the 2000 International Conference on
4-11 June 2000 Page(s):439 - 448
Digital Object Identifier 10.1109/ICSE.2000.870434

AbstractPlus | Full Text: PDF(1216 KB)   IEEE CNF
Rights and Permissions

19. **Modeling programmable logic controllers for logic verification**
Moon, I.;
Control Systems Magazine, IEEE
Volume 14, Issue 2, April 1994 Page(s):53 - 59
Digital Object Identifier 10.1109/37.272781

AbstractPlus | Full Text: PDF(520 KB)   IEEE JNL
Rights and Permissions

20. **Symbolic model checking for sequential circuit verification**
Burch, J.R.; Clarke, E.M.; Long, D.E.; McMillan, K.L.; Dill, D.L.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 13, Issue 4, April 1994 Page(s):401 - 424
Digital Object Identifier 10.1109/43.275352

AbstractPlus | Full Text: PDF(2324 KB)   IEEE JNL
Rights and Permissions

21. **Verification of speed-independent data-path circuits**
Weih, D.T.; Greenstreet, M.R.;
Computers and Digital Techniques, IEE Proceedings-
Volume 143, Issue 5, Sept. 1996 Page(s):295 - 300

AbstractPlus | Full Text: PDF(624 KB)   IEE JNL

22. **Representing TCP/IP connectivity for topological analysis of network security**
Ritchey, R.; O'Berry, B.; Noel, S.;
Computer Security Applications Conference, 2002. Proceedings. 18th Annual
9-13 Dec. 2002 Page(s):25 - 31
Digital Object Identifier 10.1109/CSAC.2002.1176275

AbstractPlus | Full Text: PDF(2338 KB)   IEEE CNF

23. Promela++: a language for constructing correct and efficient protocols
Basu, A.; Morrisett, G.; Von Eicken, T.;
INFOCOM '98. Seventeenth Annual Joint Conference of the IEEE Computer and Communications Societies. Proceedings. IEEE
Volume 2, 29 March-2 April 1998 Page(s):455 - 462 vol.2
Digital Object Identifier 10.1109/INFCOM.1998.665062

AbstractPlus | Full Text: PDF(868 KB)   IEEE CNF
Rights and Permissions

24. Formal verification of VHDL: the model checker CV
Deharbe, D.; Shankar, S.; Clarke, E.M.;
Integrated Circuit Design, 1998. Proceedings. XI Brazilian Symposium on
30 Sept.-3 Oct. 1998 Page(s):95 - 98
Digital Object Identifier 10.1109/SBCCI.1998.715418

AbstractPlus | Full Text: PDF(64 KB)   IEEE CNF
Rights and Permissions

25. Formal verification of sequential hardware: a tutorial
McFarland, M.C.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 12, Issue 5, May 1993 Page(s):633 - 654
Digital Object Identifier 10.1109/43.277609

AbstractPlus | Full Text: PDF(2132 KB)   IEEE JNL
Rights and Permissions

Help   Contact Us   Privacy & Security   IEEE.org

indexed by
⊞ Inspec*

Google
Scholar BETA
"model checker" path   1951   - 2002   Search

Advanced Scholar Searc
Scholar Preferences
Scholar Help

Scholar

Results **1 - 10** of about **1,550** for **"model checker"** path. (**0.19** seconds)

Bebop: A Symbolic **Model Checker** for Boolean Programs - group of 10 »
T Ball, SK Rajamani - spinroot.com
... correlations. We have created a **model checker** for boolean programs called Bebop .
Given ... relations Label R reachable by following **path**: Line ...
Cited by 131 - View as HTML - Web Search - BL Direct

HYTECH: a **model checker** for hybrid systems - group of 9 »
TA Henzinger, PH Ho, H Wong-Toi - International Journal on Software Tools for Technology ..., 1997 - Springer
... HyTech is a symbolic **model checker** for linear hybrid automata, a subclass of hybrid
automata that can be ana- lyzed automatically by computing with polyhedral ...
Cited by 388 - Web Search - Library Search - BL Direct

NUSMV: a new symbolic **model checker** - group of 12 »
A Cimatti, E Clarke, F Giunchiglia, M Roveri - International Journal on Software Tools for Technology ..., 2000 - Springer
... symbolic **model checker** Table 1. Definition of CTL operators $AX\alpha = \neg EX(\neg\alpha)$ For all
paths, in the next state α $EF\alpha = E[\ U\alpha]$ There exists a **path** in which ...
Cited by 100 - Web Search

A Markov Chain **Model Checker** - group of 9 »
H Hermanns, JP Katoen, J Meyer-Kayser, M Siegle - Springer
... be defined.The usual **path** quantifiers $\forall$ and $\exists$ are replaced by the probabilis ... E
MC 2), to our knowledge the first implementation of a **model checker** for CTMCs ...
Cited by 54 - Web Search - BL Direct

Model Checking and Abstraction - group of 12 »
EM Clarke, O Grumberg, DE Long - portal.acm.org
... Formulas are formed using the standard operators of linear temporal logic and two
path ... The formula 3() is true when- ever @ holds for some computation **path**. ...
Cited by 702 - Web Search - BL Direct

E cient Generation of Counterexamples and Witnesses in Symbolic Model Checking - group of 10 »
EM Clarke, O Grumberg, KL McMillan, X Zhao - portal.acm.org
... algorithm is, in fact, the one that is used in the SMV **model checker** developed at ...
Note that this algorithm guarantees a shortest **path** to a fair cycle is found. ...
Cited by 101 - Web Search - Library Search - BL Direct

A BDD-Based **Model Checker** for Recursive Programs - group of 14 »
J Esparza, S Schwoon - Springer
... if a point of a boolean program can be reached along some execution **path**. ... In this
paper we overcome this limitation by presenting a **model-checker** for boolean ...
Cited by 46 - Web Search - BL Direct

Symbolic model checking using SAT procedures instead of BDDs - group of 20 »
A Biere, A Cimatti, EM Clarke, M Fujita, Y Zhu - ieeexplore.ieee.org
... operators [1]. To simplify our discus- sion, we consider only existential LTL formulas,
ie formulas of type Ef where E is the existential **path** quantifier and f ...
Cited by 246 - Web Search - Library Search - BL Direct

The SLAM Toolkit - group of 5 »
T Ball, SK Rajamani - Springer
... **model checker** to determine the answer to this query. In this case, the answer is
"yes" and Bebop produces a (shortest) **path** p 0 leading to SLIC ERROR ...
Cited by 61 - Web Search - BL Direct

Symbolic Model Checking without BDDs - group of 27 »

A Biere, A Cimatti, EM Clarke, Y Zhu - Springer

... We have implemented a **model checker** BMC, based on bounded model checking, and preliminary ... G(x = 0). Instead of searching for an arbitrary **path**, we restrict ...

Cited by 538 - Web Search - Library Search - BL Direct

Goooooooooogle ▶

| "model checker" path | | Search |

Google Home - About Google - About Google Scholar